Talk Title: End-to-End Design for Testability
Speaker: Chen-Huan Chiang
Place: 102R, Delta Bldg

Abstract:

Design for Testability (DFT) is not only essential to ensure that an IC is manufactured correctly, but also can serve as an enabler to achieve testing at board level or even at system level. The benefits of comprehensive DFT at IC level can carry through the product life cycle from an IC all the way to the system.

From IEEE 1149.1 Standard, also known as JTAG, that was first published in 1990, to the newest test IEEE 1687 Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device (a.k.a. IJTAG), which was approved on Nov 3, 2014, we will describe various end-to-end test methodologies that we have developed within an IC or FPGA to facilitate testing of our telecommunication boards and systems.

Chen-Huan Chiang, 蔣震寰, is a Member of Technical Staff at Bell Labs, Alcatel-Lucent USA. He is also a Visiting Assistant Professor at Swarthmore College. He was an Adjunct Professor at Temple University and NJIT.

He obtained his PhD degree in Computer Engineering from the University of Southern California (USC). He graduated from NCTU (交通大學) with BS degree in Computer Engineering. His main research interests include Embedded System Design, Design for Testability at board and system levels, Built-In Self-Test, and System-On-Chip testing.

He serves IEEE Computer Society Test Technology Technical Council (TTTC) for multiple capacities and is currently the Finance Chair of TTTC. He is also the Vice General Chair of IEEE VLSI Test Symposium 2014 and 2015.

He has eight US patents and published more than 20 papers. He advised the National Science Foundation (NSF), USA, as a panelist on Design Automation forum. He is also the recipient of Bell Labs President Silver Awards in 2003, 2004 and 2005.