力成科技-劉佑信 處長

Engineer Opportunity and Challenge :
WLP Probing Technology

演講日期：104/10/19(一)
演講時間：下午 1:30-3:00
演講地點：台達館 103 室

簡歷：Clark Liu

Clark current is Director of Chip Probing Division, PowerTech Technology Inc., Taiwan and he is a SWTW committee member. He has Master of Engineering management from Tsing Hua University at Taiwan. Clark has over 20 years experience in the semiconductor testing industry. He had lead the development, with key suppliers worldwide, of 300 mm wafer probing technology starting in 1998. He also has multiple submitted and awarded patents. Now Clark′ s major focus is on WLP probing technology and business.

摘要：

WLP (Wafer Level Package) technology is being rapidly deployed by increasing end user application volumes. WLP probing technology as a manufacturing test

process needs to achieve the targets of yield, cost and performance. There has been many presentations on this topic at recent conferences including BiTS 2015 and Semiconductor Wafer Test Workshop (SWTW) 2015. This intense focus is due to the unmeet needs of the technology and customer requirements that keep pushing the probing and test industry harder. This presentation will introduce the topics of WLP probing technology, the opportunities, and the challenges. From probing technology required for WLP process technology to probe card lead times and topics in between that will drive this market will be reviewed.