

Dependable Design Techniques for Emerging Non-Volatile Memories

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摘要：

With the massive requirements of portable electronic products and communication devices, the demands of the non-volatile memories grow significantly. According to statistics, the demand for storage is doubling every 14 months and we cannot see the end point in this trend. The cost per GB drives the density of memory chips significantly. However, the miniaturization and shrinkage of transistors makes memory cells smaller and denser. It then inevitably affects the reliability and yield of the manufactured products. In this talk, I will introduce dependable design techniques to address these issues and focus on NROM and flash memory. Besides using the conventional fault replacement techniques, *fault masking* effects are also exploited to reduce the amount of spare rows/columns. In order to further enhance the fabrication yield, the *address scrambling* and the *data inversion* techniques are also presented.

簡歷：

Shyue-Kung Lu received the MS degree in 1991 from National Tsing Hua University, Hsinchu, Taiwan, and PhD degree in 1996 from National Taiwan University, Taipei, Taiwan, both in electrical engineering. From 1995 to 1998, he was an Associate Professor in the Department of Electrical Engineering, Lunghwa Junior College of Technology and Commerce, Taoyuan, Taiwan. Since 1998, he has been with the Department of Electronics Engineering, Fu Jen Catholic University, Taipei, Taiwan, where he is a professor. He also served as the Chair of the EE Department of FJU from 2006 to 2009. From 2009, he joined the Department of Electrical Engineering, National Taiwan University of Science and Technology. His research interests include the areas of VLSI testing and fault-tolerant computing, test and repair techniques for 3D stacked ICs, video coding techniques and architectures design. From 2006-2009, he served as the convener of the *Design Automation and Test Consortium* (DAT) for the Ministry of Education (MOE), Taiwan. From 2010-2014, he also served as the convener of the *Consortium of Intelligent Electronics Applications and Designs* for the MOE. Dr. Lu is a Life Member of the Taiwan IC Design Society and a member of IEEE. He is also the treasurer of IEEE Taipei Section.