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An-Yeu (Andy) Wu

An-Yeu (Andy) Wu (IEEE M'96-SM'12-F'15) received the B.S. degree from National Taiwan University in 1987, and the M.S. and Ph.D. degrees from the University of Maryland, College Park in 1992 and 1995, respectively, all in Electrical Engineering. In August 2000, he joined the faculty of the Department of Electrical Engineering and the Graduate Institute of Electronics Engineering, National Taiwan University (NTU), where he is currently a Professor. His research interests include low-power/high-performance VLSI architectures for DSP and communication applications, adaptive/multirate signal processing, reconfigurable broadband access systems and architectures, and System-on-Chip (SoC)/Network-on-Chip (NoC) platform for software/hardware co-design. He has published more than 190 refereed journal and conference papers in above research areas, together with five book chapters and 16 granted US patents.

Dr. Wu had served as the Associate Editors of leading IEEE Transactions in the circuits and systems area and signal processing area, such as IEEE TRANSACTIONS ON VERT LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS, and IEEE TRANSACTIONS ON SIGNAL PROCESSING. Dr. Wu is now serving an Associate Editor for JOURNAL of SIGNAL PROCESSING SYSTEMS (JSPS). Wu served as the General Co-Chair of 2013 International Symposium on VLSI Design, Automation & Test (VLSI-DAT), and 2013 IEEE Workshop on Signal Processing Systems (SiPS). He also served as Technical Program Co-Chair of 2014 International SoC Design Conference (ISOCC) and 2014 IEEE Asia Pacific

Conference on Circuits and Systems (APCCAS). From 2012 to 2014, he served as the Chair of VLSI Systems and Applications (VSA) Technical Committee (TC), one of the largest TCs in IEEE Circuits and Systems (CAS) Society.

From August 2007 to Dec. 2009, he was on leave from NTU and served as the Deputy General Director of SoC Technology Center (STC), Industrial Technology Research Institute (ITRI), Hsinchu, TAIWAN, supervising Parallel Core Architecture (PAC) VLIW DSP Processor and Multicore/Android SoC platform projects. In 2010, Dr. Wu received “Outstanding EE Professor Award” from The Chinese Institute of Electrical Engineering (CIEE), Taiwan. Prof. Wu is elevated to IEEE Fellow in 2015 for his contributions to “DSP algorithms and VLSI designs for communication IC/SoC.”

Thermal/Traffic-aware 3D Network-on-Chip (NoC) Designs

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Three-dimensional Network-on-Chip (3D NoC), the combination of NoC and 3D IC technology, can achieve lower latency, lower power consumption, and higher data bandwidth for efficient intra/inter-chip data exchange of chip multiprocessors (CMPs). However, due to die stacking in 3D IC, both heat conduction path and power density increase. It has been shown that NoC operations have comparable thermal impact as processing units, and significantly contributes to overall chip temperature. Besides, busy routers are prone to be overheating hotspots, which lead to the vulnerability of performance and reliability of NoC. To ensure thermal safety while avoiding huge performance degradation from the temperature constraint, new design methodologies based on smart routing schemes and proactive thermal management for thermal-/traffic-aware 3D NoC designs will be presented in this talk.