謝秉璇 教授

Ping-Hsuan Hsieh was born in Taipei, Taiwan. She received the B.S. degree from National Taiwan University in 2001, and the M.S. and Ph.D. degrees from the University of California, Los Angeles, in 2004 and 2009, respectively, all in electrical engineering.

She was an Intern with Texas Instruments in the summers from 2004 to 2006. From 2009 to 2011, she was with the IBM T.J. Watson Research Center, where she worked on the design of mixed-signal integrated circuits for high-speed serial data communication. In 2011, she joined the Electrical Engineering Department of National Tsing Hua University, Hsinchu, Taiwan, where she is currently an Assistant Professor. Her research interests include mixed-signal integrated circuit designs for high-speed electrical data communications, clocking and synchronization systems, and energy-harvesting systems for wireless sensor networks and machine-to-machine applications.

黃錫瑜 教授

◆ Education

- 1988 BS from 台大電機系
- 1992 MS from 台大電機系
- 1997 Ph.D. from ECE Dept., UC, Santa Barbara

◆ Working Experience

- Oct. 1997 – July 1998 National Semi, Santa Clara, USA
- Aug. 1998 – July 1999 世大 (後併入台積電)
- Aug. 1999 – now, 清華電機系
- (Current: 電機系教授兼任清大積體電路設計中心主任)

◆ Start-up Experience

兆心科技 (2007-2012)

(主要產品是 cell-based PLL compiler 和快又準的功率消耗評估軟體)

◆ Research Interests and Others

Dr. Huang's previous research topics include formal verification, power estimation, fault diagnosis, and resilient nanometer SRAM Design and its complier. Recently, his research is more concentrated on all-digital timing circuit design, such as all-digital phase-locked loop (PLL), all-digital delay-locked loop (DLL), time-to-digital converter (TDC), and their applications to parametric fault testing and reliability enhancement for 3D-ICs. Dr. Huang has published more than 120 refereed technical papers, including 33 IEEE journal papers. He received the best-presentation award in 2006 and the best-paper award in 2013 from Int'l Symposium on VLSI, Design, Automation, and Test. He is now serving as an Associate Editor for IEEE Trans. on Computers.

All-Digital Phase-Locked Loop and Its Compiler

(第一部分) Speaker: Prof. Ping-Hsuan Hsieh

Digital phase---locked loops (DPLLs) have drawn a great deal of interest in the recent decade. The main driver for this design effort is the difficulties in analog circuit design with technology scaling. Applications that require stability and performance across a wide operating frequency range such as DVFS, spread---spectrum I/O, and multi---use IP cells have even more challenging design requirements. Instead of seeking more sophisticated yet likely more complicated analog circuit techniques, DPLLs take advantage of technology scaling by digitizing the clock signal and using a fully digital loop filter.

In this talk, we will first present a DPLL used for GHz clock generation in modern digital systems with >100x range of operating frequency. The DPLL uses phase selection and interpolation as the DCO for low jitter performance and wide operating frequency range. A bandwidth---tracking technique that uses replica delay cells in the DCO and the PD is introduced to enable stable operation across the frequency range without calibration. The proposed design achieves an output frequency up to 1.8 GHz in a 65---nm CMOS technology. Nearly constant damping factor and the tracking of the loop bandwidth to reference frequency are shown with a dynamic sweep of 8 reference frequency range (from 28 MHz to 225 MHz with core frequency of 3.6 GHz). The prototype consumes 220 mW at 1.6 GHz with the measured rms/pp jitter of 2.63/22.2 ps.

We will also cover a few more design examples to show the various advantages of such digital implementations.

All-Digital Phase-Locked Loop and Its Compiler

(第二部分) Speaker: Prof. Shi-Yu Huang

We will present a Cell-Based PLL Compiler (named eClock). This compiler, as the first of its kind to our knowledge, can help the designers to generate a PLL instance in just minutes. For certain types of application (e.g., clock signal generation), automatically complied cell-based PLLs could offer the benefits of smaller area, lower power consumption, and easier migration to new process technologies as compared to its analog counterpart.

Also, we will introduce a state-of-the-art delay characterization method for interconnects, which allows an IC design and/or integrator to quantify the delays across the bus signals and/or die-to-die interconnects in silicon. It is useful in many aspects, including timing validation, small delay testing, process tracking, yield diagnosis, and returned product debugging.